

## escICU - Hyperspectral Camera Instrument Control Unit

**Camera ICU** is a powerful universal payload computer for new space satellite platforms and compatible with cubesat platforms. The dimensions are matched with the PC104 form factor.

The powerful System on Chip combining multi-core processor and programmable logic array allows efficient and real-time execution of complex algorithms to process raw data on-board, thus reducing space to ground communications bandwidth needs.

Integrated mass memory for storage of acquired data allows to use of the ICU without need of platform data storage. Data is accessible via Cubesat Space Protocol or ECSS PUS-C via platform communication bus.

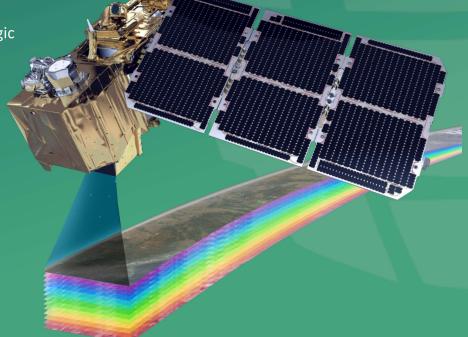
Latch-up protection of the ICU and imaging sensor is assured by constant current monitoring and several mitigation techniques.

## **Key features**

- Four 64-bit Linux capable user cores + one supervisor core
- Programmable logic array for image sensor readout and functionality extension
- Multiple image sensors readout possible
- Warm/cold redundancy support
- On-board current, voltage and temperature monitoring
- Latch-up monitoring
- Onboard data storage

• User script support for ICU control and data pre-processing (MicroPython)

 Software and programmable logic upgradable





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## **Technical Specifications**

| General              |  | Interfaces              |                                     |
|----------------------|--|-------------------------|-------------------------------------|
| Processor            | 5x RISC-V 64-bit                       | CAN                     | 2x                                  |
| Logic blocks         | 254 K                                  | RS422/RS-485            | 2x                                  |
| Processor clock      | up to 625 MHz                          | UART 3.3 V              | 1x                                  |
| Program. logic clock | up to 343 MHz                          | PPS (RS-422)            | 1x                                  |
| DRAM CPU             | 1024 MB (ECC)                          | GPIO 3.3 V logic        | 8x                                  |
| 51 G. G              | (2048 MB optional)                     | JTAG for SoC            | 1x                                  |
| DRAM FPGA            | 1024 MB (ECC)<br>(2048 MB optional)    | Ethernet up to<br>1Gbps | 1x (2x optional)                    |
| NVM (program)        | 128 MB (redundant)                     |                         | up to 16x lanes                     |
| NVM (configuration)  | 16 MB (redundant)                      | Image sensor            | (SerDes 12.7 Gbps)                  |
| Mass storage         | 2 GB SLC NAND<br>(up to 32GB optional) |                         | up to 36x pairs<br>(LVDS 1250 Mbps) |
| Power supply         | 5 V ± 5%                               | Size and Weight         |                                     |
| rower supply         | (28 V optional)                        | Length                  | 96 mm                               |
| Power supply         | up to 10 W                             | Width                   | 91 mm                               |
| Op. temperature      | -30 °C to +60 °C                       | Height                  | 35 mm (TBC)                         |
| Non-op. temperature  | -40 °C to +85 °C                       | Mass                    | 350 g (TBC)                         |



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